UNIVERSIDADE TECNOLÓGICA FEDERAL DO PARANÁ
CURSO DE ENGENHARIA DE COMPUTAÇÃO

EDUARDO FELIPE WEBER

PROJETO E MODELO DE UM CONVERSOR *BOOST INTERLEAVED*

TRABALHO DE CONCLUSÃO DE CURSO

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Trabalho de Conclusão de Curso apresentado ao Curso de Engenharia de Computação da Universidade Tecnológica Federal do Paraná - UTFPR Campus Toledo, como requisito parcial para a obtenção do título de Bacharel em Engenharia de Computação.

Orientador: Prof. Dr. Cassius Rossi de Aguiar
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TERMO DE APROVAÇÃO

Título do Trabalho de Conclusão de Curso Nº 02

Projeto e modelo de um conversor *boost interleaved*

por

Eduardo Felipe Weber

Esse Trabalho de Conclusão de Curso foi apresentado às **14h00 do dia 27 de novembro de 2019** como **requisito parcial** para a obtenção do título de **Bacharel em Engenharia de Computação**. Após deliberação da Banca Examinadora, composta pelos professores abaixo assinados, o trabalho foi considerado **APROVADO**.

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O termo de aprovação assinado encontra-se na coordenação do curso

Toledo, 27 de novembro de 2019

RESUMO

WEBER, Eduardo F.. Projeto e modelo de um conversor *boost interleaved*. 2019. 0 f. Trabalho de Conclusão de Curso – Curso de Engenharia de Computação, Universidade Tecnológica Federal do Paraná. Toledo, 2019.

O objetivo deste trabalho é analisar e projetar um um conversor elevador de tensão utilizando a técnica *interleaved*, que melhora a resposta transitória da carga, tem melhor dissipação de calor e menos estresse nos semicondutores. Para representar o conversor *boost interleaved* em um modelo matemático, é utilizada a representação em espaço de estados, no qual é considerada a resistência parasita dos indutores e semicondutores. Nesse contexto, o conversor *boost interleaved* é controlado usando uma estrutura em cascata com o controle de corrente nos indutores no circuito interno e o controle de tensão do link CC no circuito externo. Após investigar a resposta dos controladores no domínio da frequência, indicando a estabilidade do sistema, o conversor é validado por simulações e medições experimentais destacando o correto funcionamento do sistema, atingindo a tensão desejada com pequena amplitude de ondulação residual.
Palavras-chave: Coversor CC-CC. Eletrônica de Potência. Fotovoltaico.

ABSTRACT

WEBER, Eduardo F.. Model and Design of an Interleaved Boost Converter. 2019. 0 f. Trabalho de Conclusão de Curso – Curso de Engenharia de Computação, Universidade Tecnológica Federal do Paraná. Toledo, 2019.

The aim of this paper is to analyze and design a boost power converter utilizing the interleaved technique, which improves the load transient response, provides better heat dissipation and less stress on the semiconductors. To represent the interleaved boost converter in a mathematical model, its state space representation is used, where the parasitic resistance of the inductors and semiconductors is considered. In this context, the interleaved boost converter is controlled using a cascade structure with the input current on the inductors in the inner loop and the dc-link voltage in the outer loop. After investigating the response of the controllers in the frequency domain, indicating the stability of the system, the converter is validated by simulations and by experimental measurements highlighting the correct operation of the system, reaching the desired voltage with small residual ripple amplitude.

Keywords: DC-DC Converter. Power Electronics. Photovoltaic.

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LISTA DE ABREVIATURAS E SIGLAS

PI	*Proportional Integral*
IBC	*Interleaved Boost Converter*
MMP	*Maximum Power Point*
KCL	*Kirchhoff's Current Law*
KVL	*Kirchhoff's Voltage Law*
DSP	*Digital Signal Processor*
PWM	*Pulse Width Modulation*

SUMÁRIO

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Model and Design of an Interleaved Boost Converter

Eduardo Felipe Weber · Cassius Rossi de Aguiar

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Abstract The aim of this paper is to analyze and design a boost power converter utilizing the interleaved technique, which improves the load transient response, provides better heat dissipation and less stress on the semiconductors. To represent the interleaved boost converter in a mathematical model, its state space representation is used, where the parasitic resistance of the inductors and semiconductors is considered. In this context, the interleaved boost converter is controlled using a cascade structure with the input current on the inductors in the inner loop and the dc-link voltage in the outer loop. After investigating the response of the controllers in the frequency domain, indicating the stability of the system, the converter is validated by simulations and by experimental measurements highlighting the correct operation of the system, reaching the desired voltage with small residual ripple amplitude.

Keywords Interleaved Boost Converter · Power Electronics · Photovoltaic Energy

1 Introduction

The low-voltage renewable energy sources require, usually, the utilization of different topologies of power electronic converters to adjust its output voltage and current. Mostly solar panels operate in medium to low voltage output and require dc/dc boost converters with high voltage gain to be connected to the grid. Taking this into consideration, the main factors that affect efficiency and gain are the correct topology and the accounting for parasitic losses as described in (Thao et al., 2012).

A step-up converter, fit for a renewable energy system that needs high voltage gain, is proposed in (Liu et al., 2015). This converter utilizes two switches, one voltage multiplier cell for each arm and three winding coupled inductors. The utilization of two switches reduces the voltage and current stresses on the semiconductors. Another example is the interleaved boost converter with voltage multiplier proposed in (Franco et al., 2003; Gul, 2003), and modeled in (Spiazzi et al., 2012) which brings many advantages like the use of voltage multiplier cells and specifically the interleaved technique.

Among the most know topologies of dc/dc converter, the interleaved technique introduces numerous benefits, like, current sharing between the arms, use of cheaper semiconductor, reduction of the input current ripple (Thounthong et al., 2009; Fekri et al., 2017; Maalandish et al., 2017), reduced inductors, improvement of the converter efficiency and a better thermal distribution (Jang et al., 2013; Cheng et al., 2013; Ang and Oliva, 2010).

Based on the introduced arguments, this work presents a mathematical model, analysis, closed-loop control and simulation of a two-phase interleaved boost converter (IBC) taking into account the parasitic resistances of the passive components and switches. The employment of multiplier cells was not considered once the targeted voltage gain was achieved without their use.

This paper is organized as follows: in Section II the interleaved technique and the proposed IBC are described; in Section III it is shown the procedure of the photovoltaic device linearization; in Section IV the

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state-space model is made by subdividing the full operation cycle into multiple subintervals and analysing each equivalent circuit; then on Section V the average model and small signal analysis is derived; in Section VI it is made the control analysis of the IBC for its utilization on Section VII where the converter is simulated; on section VIII its shown the experimental results; and lastly, Section IX describes the conclusions made from the execution of this project.

2 Interleaved boost converter

The interleaved technique is the combination of two or more converters in parallel, as shown in Figure (1). The switching of the phases operates in a manner that the current distributes itself between the N phases with a delay of $360^o/N$ between each one, thus the resulting switching frequency will be proportional to the number of phases N.

By the fact that the current splits across the arms of the phases, the currents will be reduced in each arm. Therefore, inductors and semiconductors maximum ratings can also be reduced, which implies in better costs. Furthermore, it is possible to arrange the components with better distribution, resulting in more efficient heat dissipation.

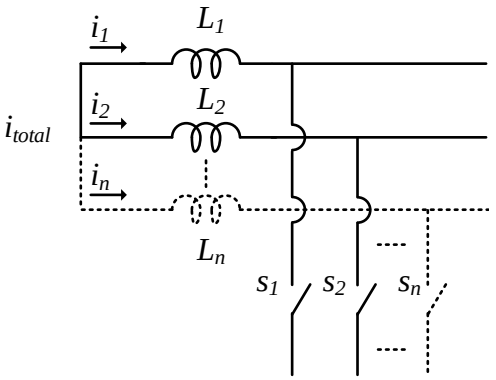

Fig. 1 Representation of an interleaved technique of N phases.

In this project it is developed an interleaved boost converter with two phases, utilizing an arrangement of solar panels as input, using two switches and a load represented as a resistor R_L (Figure 2). The goal is to develop a IBC that supplies 200 V and up to 1 kW of power.

As stated previously the parasitic losses affect the efficiency of the converter, thus, they shall be accounted in order to be compensated. $R_{C_{in}}$ is the parasitic resistance of the input capacitor C_{in}, R_{L_1}, R_{L_2} the parasitic resistances of the inductors L_1 and L_2 respectively and, at last, the intrinsic losses R_{S_1}, R_{S_2} from the switches S_1 and S_2.

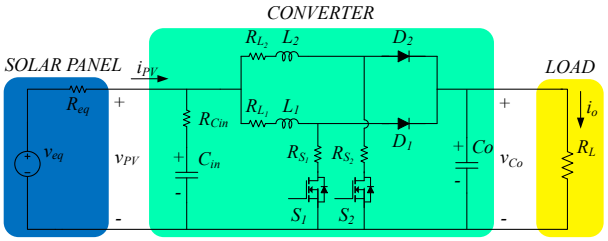

Fig. 2 Proposed boost interleaved converter.

In the following sections the development process will be described step by step, starting with the linearization of the simulated arrangement of solar panels, then describing the space-state model, the average model, the small signal analyses to acquire the transfer functions, the control topology and at last the simulation and experimental results.

3 Linearization of the photovoltaic device

Instead of utilizing an ideal power source to represent the arrangement of solar panels it is preferable to find an equation that is closer to the operation of a real solar panel (Villalva, 2010). However, the equation that describes a photovoltaic device is not linear. Therefore it is necessary to linearize a point in the curve of current by voltage from the solar panel, thereby, finding an equivalent circuit that can be represented in the model of the system. The chosen point to do it is the point where the solar panel operates with its maximum power (MPP).

The solar panel that will be simulated in this project is the 280W model CS6K280P from Canadian Solar. It will be arranged using four solar panels, being two in series and this group in parallel with another two in series as shown in the Figure (3).

Figure (4) represents the curve of the current by the voltage of one solar panel. The highlighted point is where the solar panel operates at its full capacity, generating its maximum power output. The tangent line over the point defines how the linearization of the curve is made.

The conductance of the panels arrangement g, linearized in the chosen point in the position (X, Y), it is calculated in the equation (1), where (I, V) is a point inside the tangent line.

$$g = \frac{\Delta Y}{\Delta X} = \frac{i_{PV} - I}{v_{PV} - V} = \frac{1}{R_{eq}} \tag{1}$$

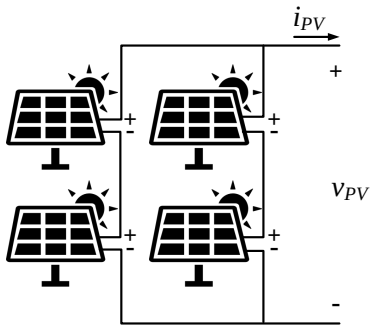

Fig. 3 Arrangement of the solar panels.

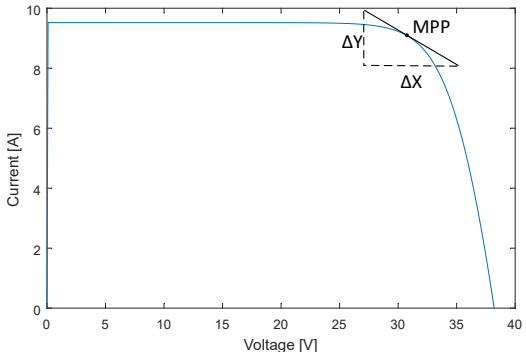

Fig. 4 Example of curve of the current in function of the voltage of a solar panel.

Rearranging (1) is obtained (2) that represents the linear model of the tangent line on the chosen point.

$$i_{PV} = (-gV + I) + gv_{PV} \tag{2}$$

Thereby, it is possible to represent the linearized solar panel as an equivalent circuit as pictured in the Figure (5)

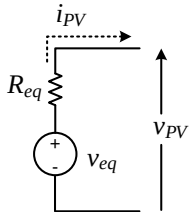

Fig. 5 Equivalent circuit to represent a solar panel.

Analyzing the circuit in the Figure (5), the equations (3) and (4) are obtained representing the equivalent resistance and equivalent voltage of the solar panel respectively.

$$R_{eq} = -\frac{1}{g} \tag{3}$$

$$V_{eq} = V - \frac{I}{g} \tag{4}$$

With this linearized model, the following analysis for the project of controllers will be facilitated and, furthermore, this model describes the operation of the solar panel satisfactorily.

4 IBC state-space model

As the aim of this project is to control the IBC in closed-loop, it is necessary to represent it mathematically. To do so, the state-space model was developed in order to describe the IBC. The space-state modeling is based on the works of (Aguiar, 2017) and (Fuzato, 2015).

The semiconductors are switching with 180° apart, and considering the full period as T_s and the period that one switch is closed as kT_s there will be four different subintervals: k_1T_s, where the switches S_1 and S_2 are closed; k_2T_s, when the switch S_2 keeps closed and the switch S_1 opens; k_3T_s when, again, both switches are closed; and lastly, k_4T_s when the switch S_2 opens and the switch S_1 remains closed.

During the first subinterval both inductors, L_1 and L_2, are charging. When the subinterval finishes and the second subinterval starts the inductor L_1 discharges its energy on the load R_L, then on the third interval, the inductor L_1 restart charging, at the same time as L_2. On the final subinterval, the inductor L_2 discharges its energy on the load R_L, and the cycle repeats. The Figure (6) represents the correlation between the flow of current through the inductors and the state of the switches.

To obtain the state-space model of the IBC the state vector will be assumed as (5), the input vector as (6), and the output vector as (7).

$$x = \begin{bmatrix} i_{L_1} & i_{L_2} & v_{C_{in}} & v_{Co} \end{bmatrix}^T \tag{5}$$

$$u = \begin{bmatrix} v_{PV} \\ i_o \end{bmatrix} \tag{6}$$

$$y = \begin{bmatrix} i_{L_1} + i_{L_2} \\ v_{Co} \end{bmatrix} \tag{7}$$

To proceed with the following analysis, such as average model and small-signal analysis, it is necessary to model the equivalent circuit of each subinterval.

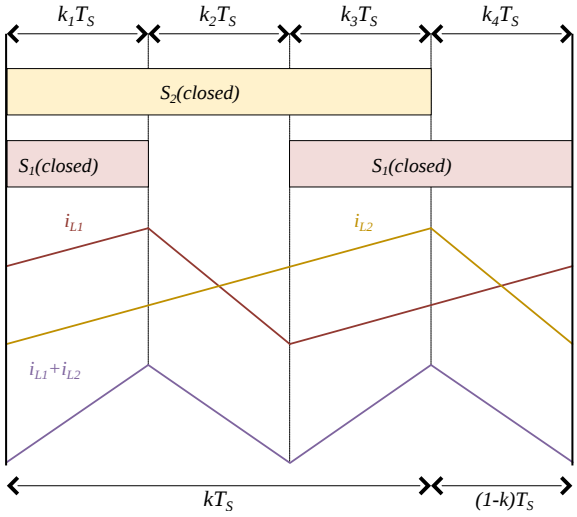

Fig. 6 Correlation between the flow of current through the inductors and the state of the switches, adapted from Fuzato (2015)

4.1 First Subinterval

In the first subinterval, both switches are closed and both diodes are reversely biased, as represented in the Figure (7).

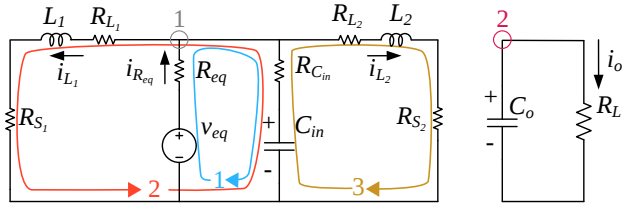

Fig. 7 Equivalent circuit of the first subinterval.

Applying KCL (Kirchhoff's Current Law) on the node (1) in (8) is obtained, and using KVL (Kirchhoff's Voltage Law) on the loop (1) it is possible to obtain the equation (9).

$$i_{L_1} + i_{L_2} + C_{in}\frac{dv_{C_{in}}}{dt} = i_{R_{eq}} \tag{8}$$

$$i_{R_{eq}} = \left[v_{eq} - (v_{C_{in}} + C_{in}\frac{dv_{C_{in}}}{dt}R_{C_{in}})\right]\frac{1}{R_{eq}} \tag{9}$$

Applying (9) in (8), the following equation is obtained:

$$\begin{aligned} &i_{L_1} + i_{L_2} + C_{in}\frac{dv_{C_{in}}}{dt} = \\ &\left(v_{eq} - v_{C_{in}} - C_{in}\frac{dv_{C_{in}}}{dt}R_{C_{in}}\right)\frac{1}{R_{eq}} \end{aligned} \tag{10}$$

Now, isolating $\frac{dv_{C_{in}}}{dt}$ in the equation (10) it is possible to obtain:

$$\frac{dv_{C_{in}}}{dt} = \frac{-R_{eq}(i_{L_1} + i_{L_2}) + v_{eq} - v_{C_{in}}}{C_{in}(R_{eq} + R_{C_{in}})} \tag{11}$$

Applying KVL in the loop (2), (12)is obtained. Applying (11) on (12) and isolating $\frac{di_{L_1}}{dt}$ (13) is obtained.

$$\begin{aligned} &-v_{C_{in}} - R_{C_{in}}C_{in}\frac{dv_{C_{in}}}{dt} + \\ &L_1\frac{di_{L_1}}{dt} + i_{L_1}(R_{L_1} + R_{S_1}) = 0 \end{aligned} \tag{12}$$

$$\begin{aligned} \frac{di_{L_1}}{dt} = &+ v_{C_{in}}\left[\frac{R_{eq}}{(R_{eq} + R_{C_{in}})L_1}\right] \\ &+ v_{eq}\left[\frac{R_{C_{in}}}{(R_{eq} + R_{C_{in}})L_1}\right] \\ &+ i_{L_1}\left[-\frac{R_{L_1}}{L_1} - \frac{R_{S_1}}{L_1} - \frac{R_{C_{in}}R_{eq}}{(R_{eq} + R_{C_{in}})L_1}\right] \\ &+ i_{L_2}\left[-\frac{R_{C_{in}}R_{eq}}{(R_{eq} + R_{C_{in}})L_1}\right] \end{aligned} \tag{13}$$

Repeating the same process in the loop (3), the following equations are found:

$$\begin{aligned} &- v_{C_{in}} - R_{C_{in}}C_{in}\frac{dv_{C_{in}}}{dt} + \\ &L_2\frac{di_{L_2}}{dt} + i_{L_2}(R_{L_2} + R_{S_2}) = 0 \end{aligned} \tag{14}$$

$$\begin{aligned} \frac{di_{L_2}}{dt} = &+ v_{C_{in}}\left[\frac{R_{eq}}{(R_{eq} + R_{C_{in}})L_2}\right] \\ &+ v_{eq}\left[\frac{R_{C_{in}}}{(R_{eq} + R_{C_{in}})L_2}\right] \\ &+ i_{L_1}\left[-\frac{R_{C_{in}}R_{eq}}{(R_{eq} + R_{C_{in}})L_2}\right] \\ &+ i_{L_2}\left[-\frac{R_{L_2}}{L_2} - \frac{R_{S_2}}{L_2} - \frac{R_{C_{in}}R_{eq}}{(R_{eq} + R_{C_{in}})L_2}\right] \end{aligned} \tag{15}$$

At last, applying KCL in the node (2) results in the following equation:

$$\frac{dv_{C_o}}{dt} = \frac{v_{C_o}}{R_L C_o} \tag{16}$$

Now with the equations (11), (13), (15), (16) and assuming that $\alpha = (R_{eq} + R_{C_{in}})$ it is possible to build the matrices $\boldsymbol{A_1}$ and $\boldsymbol{B_1}$, represented by the following equations, respectively on the matrices (18) and (17):

$$\boldsymbol{A_1} = \begin{bmatrix} \frac{-R_{L_1}\alpha - R_{S_1}\alpha - R_{C_{in}}R_{eq}}{\alpha L_1} & -\frac{R_{C_{in}}R_{eq}}{\alpha L_1} & \frac{R_{eq}}{\alpha L_1} & 0 \\ -\frac{R_{C_{in}}R_{eq}}{\alpha L_2} & \frac{-R_{L_2}\alpha - R_{S_2}\alpha - R_{C_{in}}R_{eq}}{\alpha L_2} & \frac{R_{eq}}{\alpha L_2} & 0 \\ -\frac{R_{eq}}{C_{in}\alpha} & -\frac{R_{eq}}{C_{in}\alpha} & -\frac{1}{C_{in}\alpha} & 0 \\ 0 & 0 & 0 & -\frac{1}{R_L C_o} \end{bmatrix} \tag{18}$$

$$\boldsymbol{B_1} = \begin{bmatrix} \frac{R_{C_{in}}}{\alpha L_1} & 0 \\ \frac{R_{C_{in}}}{\alpha L_2} & 0 \\ \frac{1}{\alpha C_{in}} & 0 \\ 0 & 0 \end{bmatrix} \tag{17}$$

4.2 Second Subinterval

In the second subinterval the switch S_2 remains closed, but now the switch S_1 opens and the diode D_1 is directly biased as shown in the equivalent circuit of the Figure (8).

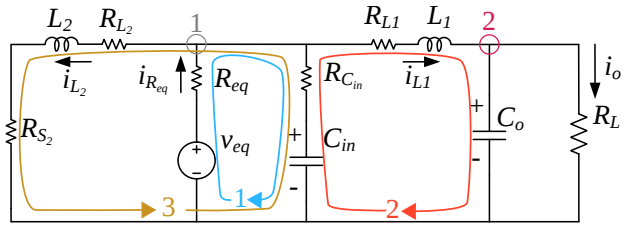

Fig. 8 Equivalent circuit of the second subinterval.

After applying KCL at the node (1) and KVL in the loop (1), relations (19) and (20), are derived. Afterwards, relation (21) is obtained by applying (19) on (20).

$$i_{L_1} + i_{L_2} + C_{in}\frac{dv_{C_{in}}}{dt} = i_{R_{eq}} \tag{19}$$

$$i_{R_{eq}} = \left[v_{eq} - (v_{C_{in}} + C_{in}\frac{dv_{C_{in}}}{dt}R_{C_{in}})\right]\frac{1}{R_{eq}} \tag{20}$$

$$\begin{aligned} &i_{L_1} + i_{L_2} + C_{in}\frac{dv_{C_{in}}}{dt} = \\ &\left(v_{eq} - v_{C_{in}} - C_{in}\frac{dv_{C_{in}}}{dt}R_{C_{in}}\right)\frac{1}{R_{eq}} \end{aligned} \tag{21}$$

Now, (22) is obtained by rearranging (21) and isolating $\frac{dvC_{in}}{dt}$:

$$\frac{dv_{C_{in}}}{dt} = \frac{-R_{eq}(i_{L_1} + I_{L_2}) + V_{eq} - v_{C_{in}}}{C_{in}(R_{eq} + R_{C_{in}})} \tag{22}$$

After applying KVL in the loop (2), relation (23) is derived. Afterwards, relation (24) is obtained by applying (22) on (23) and isolating $\frac{di_{L_1}}{dt}$.

$$\begin{aligned} &-v_{C_{in}} - R_{C_{in}}C_{in}\frac{dv_{C_{in}}}{dt} + \\ &L_1\frac{di_{L_1}}{dt} + i_{L_1}R_{L_1} + v_{Co} = 0 \end{aligned} \tag{23}$$

$$\begin{aligned} \frac{di_{L_1}}{dt} = &+ v_{C_{in}}\left[\frac{R_{eq}}{(R_{eq}+R_{C_{in}})L_1}\right] \\ &+ v_{eq}\left[\frac{R_{C_{in}}}{(R_{eq}+R_{C_{in}})L_1}\right] \\ &+ i_{L_1}\left[\frac{-R_{L_1}(R_{eq}+R_{C_{in}}) - R_{C_{in}}R_{eq}}{(R_{eq}+R_{C_{in}})L_1}\right] \\ &+ i_{L_2}\left[\frac{-R_{C_{in}}R_{eq}}{(R_{eq}+R_{C_{in}})L_1}\right] + v_{Co}\left[-\frac{1}{L_1}\right] \end{aligned} \tag{24}$$

Repeating this process for the loop (3) it is possible to obtain the following equations:

$$\begin{aligned} &-v_{C_{in}} - R_{C_{in}}C_{in}\frac{dv_{C_{in}}}{dt} + \\ &L_2\frac{di_{L_2}}{dt} + i_{L_2}(R_{L_2} + R_{S_2}) = 0 \end{aligned} \tag{25}$$

$$\begin{aligned} \frac{di_{L_2}}{dt} = &+ v_{C_{in}}\left[\frac{R_{eq}}{(R_{eq}+R_{C_{in}})L_2}\right] \\ &+ v_{eq}\left[\frac{R_{C_{in}}}{(R_{eq}+R_{C_{in}})L_2}\right] \\ &+ i_{L_1}\left[-\frac{R_{C_{in}}R_{eq}}{(R_{eq}+R_{C_{in}})L_2}\right] \\ &+ i_{L_2}\left[-\frac{R_{L_2}}{L_2} - \frac{R_{S_2}}{L_2} - \frac{C_{in}R_{eq}}{(R_{eq}+R_{C_{in}})L_2}\right] \end{aligned} \tag{26}$$

Now performing KCL at the node (2), the following equation is found:

$$\frac{dv_{Co}}{dt} = \frac{i_{L_1}}{C_o} - \frac{v_{Co}}{R_L C_o} \tag{27}$$

$$\boldsymbol{A_2} = \begin{bmatrix} \frac{-R_{L_1}\alpha - R_{C_{in}}R_{eq}}{\alpha L_1} & \frac{-R_{C_{in}}R_{eq}}{\alpha L_1} & \frac{R_e q}{\alpha L_1} & \frac{-1}{L_1} \\ \frac{-R_{eq}R_{C_{in}}}{\alpha L_2} & \frac{-(R_{L_2}+R_{S_2})\alpha - R_{eq}R_{C_{in}}}{\alpha L_2} & \frac{R_{eq}}{\alpha L_2} & 0 \\ -\frac{R_{eq}}{C_{in}\alpha} & -\frac{R_{eq}}{C_{in}\alpha} & -\frac{1}{C_{in}\alpha} & 0 \\ \frac{1}{C_O} & 0 & 0 & -\frac{1}{R_L C_o} \end{bmatrix} \tag{28}$$

$\boldsymbol{A_2}$ and $\boldsymbol{B_2}$ are obtained at (28) and (29) as result of rearranging (22), (24), (26), and (27) in a matrix form.

$$\boldsymbol{B_2} = \begin{bmatrix} \frac{R_{C_{in}}}{\alpha L_1} & 0 \\ \frac{R_{C_{in}}}{\alpha L_2} & 0 \\ \frac{1}{\alpha C_{in}} & 0 \\ 0 & 0 \end{bmatrix} \tag{29}$$

4.3 Third Subinterval

In this subinterval both of the switches are closed and both diodes are reverse biased in the same manner they were on the first subinterval, hence it is possible to say that both subintervals are equal. Therefore $\boldsymbol{A_1} = \boldsymbol{A_3}$ and $\boldsymbol{B_1} = \boldsymbol{B_3}$.

4.4 Fourth Subinterval

Now the S_1 switch mantains itself closed while the switch S_2 opens and the diode D_1 is directly polarized, as shown in figure (9).

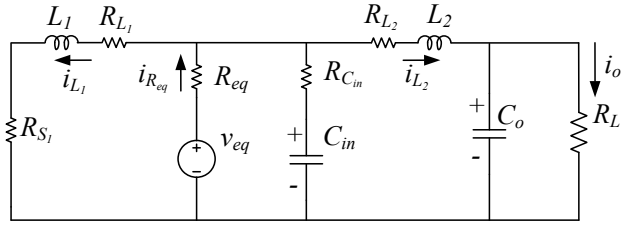

Fig. 9 Equivalent circuit of the fourth subinterval.

This subinterval closely resembles to the second subinterval, however where there is an "1" here on the second subinterval there is an "2" reciprocally. Therefore, it is possible to modify the equations (22), (24), (26), and (27) replacing L_1 for L_2, S_1 for S_2 and vice versa. Thus, it is possible to acquire the equations of the fourth subinterval with the same relations aforementioned. The resulting equations are given as follows:

$$\frac{dv_{C_{in}}}{dt} = \frac{-R_{eq}(i_{L_2} + i_{L_1}) + V_{eq} - v_{C_{in}}}{C_{in}(R_{eq} + R_{C_{in}})} \tag{30}$$

$$\begin{aligned} \frac{di_{L_2}}{dt} =& + v_{C_{in}}\left[\frac{R_{eq}}{(R_{eq}+R_{C_{in}})L_2}\right] \\ &+ v_{eq}\left[\frac{R_{C_{in}}}{(R_{eq}+R_{C_{in}})L_2}\right] \\ &+ i_{L_2}\left[\frac{-R_{L_2}(R_{eq}+R_{C_{in}}) - R_{C_{in}}R_{eq}}{(R_{eq}+R_{C_{in}})L_2}\right] \\ &+ i_{L_1}\left[\frac{-R_{C_{in}}R_{eq}}{(R_{eq}+R_{C_{in}})L_2}\right] + v_{Co}\left[-\frac{1}{L_2}\right] \end{aligned} \tag{31}$$

$$\begin{aligned} \frac{di_{L_1}}{dt} =& + v_{C_{in}}\left[\frac{R_{eq}}{(R_{eq}+R_{C_{in}})L_1}\right] \\ &+ v_{eq}\left[\frac{R_{C_{in}}}{(R_{eq}+R_{C_{in}})L_1}\right] \\ &+ i_{L_2}\left[-\frac{R_{C_{in}}R_{eq}}{(R_{eq}+R_{C_{in}})L_1}\right] \\ &+ i_{L_1}\left[-\frac{R_{L_1}}{L_1} - \frac{R_{S_1}}{L_1} - \frac{C_{in}R_{eq}}{(R_{eq}+R_{C_{in}})L_1}\right] \end{aligned} \tag{32}$$

$$\frac{dv_{Co}}{dt} = \frac{i_{L_2}}{C_o} - \frac{v_{Co}}{R_L C_o} \tag{33}$$

Rearranging the latter equations into a matricial form it is possible to form the matrices represented in (35) and (34).

$$\boldsymbol{B_4} = \begin{bmatrix} \frac{R_{C_{in}}}{\alpha L_1} & 0 \\ \frac{R_{C_{in}}}{\alpha L_2} & 0 \\ \frac{1}{\alpha C_{in}} & 0 \\ 0 & 0 \end{bmatrix} \tag{35}$$

5 IBC small-signal model

In this section the average and small signal models are investigated. The switching intervals of the circuit are defined by the present switches and diodes on the circuit. Every one of the subintervals with its equivalent circuit resultant from the switching was modeled in the former section.

Thus, after acquiring the state-space model matrices of all subintervals, the average matrix that represents the full interval can be found by the combination of

$$\boldsymbol{A_4} = \begin{bmatrix} \frac{-(R_{L_1}+R_{S_1})\alpha - R_{eq}R_{C_{in}}}{\alpha L_1} & \frac{-R_{eq}R_{C_{in}}}{\alpha L_1} & \frac{R_{eq}}{\alpha L_1} & 0 \\ \frac{-R_{C_{in}}R_{eq}}{\alpha L_2} & \frac{-R_{L_2}\alpha - R_{C_{in}}R_{eq}}{\alpha L_2} & \frac{R_{eq}}{\alpha L_2} & \frac{-1}{L_2} \\ -\frac{R_{eq}}{C_{in}\alpha} & -\frac{R_{eq}}{C_{in}\alpha} & -\frac{1}{C_{in}\alpha} & 0 \\ \frac{1}{C_O} & 0 & 0 & -\frac{1}{R_L C_o} \end{bmatrix} \tag{34}$$

the obtained matrices weighted by its relative period of every one of the switching subintervals, as shown in the subsequent equation:

$$\dot{\boldsymbol{x}} = \left(\sum_{i=1}^{4} \boldsymbol{A_i} k_i\right)\boldsymbol{x} + \left(\sum_{i=1}^{4} \boldsymbol{B_i} k_i\right)\boldsymbol{u} \tag{36}$$

Recalling Figure (6), and observing the switching angle offset of 180 degrees, it is possible to state that $k_1T_S + k_2T_S = \frac{T_S}{2}$ and that $k_3T_S + k_4T_S = \frac{T_S}{2}$. It is also possible to affirm that k_2 and k_4 are equal to $(1-k)$, once that it is the interval in which every one of the switches remain open. Therefore $k_1 = k_3 = \frac{1}{2} - (1-k) = k - \frac{1}{2}$. Thus the equation that describes the full interval of the IBC is:

$$\begin{aligned} \boldsymbol{A} = \sum_{i=1}^{4} \boldsymbol{A_i} k_i = \boldsymbol{A_1}(k - \frac{1}{2}) + \boldsymbol{A_2}(1-k) + \\ \boldsymbol{A_3}(k - \frac{1}{2}) + \boldsymbol{A_4}(1-k) \end{aligned} \tag{37}$$

$$\boldsymbol{A} = (-\boldsymbol{A_1} + \boldsymbol{A_2} + \boldsymbol{A_4}) + k(2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4}) \tag{38}$$

As the $\boldsymbol{B}$ matrices are all equal, its weighted value is invariant:

$$\boldsymbol{B} = \boldsymbol{B_1} \tag{39}$$

Considering that this converter has an non-linear behaviour and that any perturbance in the input vector $\boldsymbol{u} = \boldsymbol{U} + \hat{\boldsymbol{u}}$, where $\boldsymbol{U}$ is the average dc value and $\hat{\boldsymbol{u}}$ is the perturbance, will in a similar manner spread to the state vector $\boldsymbol{x} = \boldsymbol{X} + \hat{\boldsymbol{x}}$ and consequently to the output vector $\boldsymbol{y} = \boldsymbol{Y} + \hat{\boldsymbol{y}}$, and thus the duty cycle k will change from cycle to cycle around a linearization point, as represented by $k = K + \hat{k}$ where K is the average value in steady state and $\hat{k}$ is perturbance around the linearization point. Without the effect of the perturbance the system can be described as:

$$\begin{aligned} \dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u} = \\ + [(-\boldsymbol{A_1} + \boldsymbol{A_2} + \boldsymbol{A_4}) + k(2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4})]\boldsymbol{x} \\ + \boldsymbol{B}\boldsymbol{u} \end{aligned} \tag{40}$$

Inserting the perturbation in (40):

$$\begin{aligned} \dot{\boldsymbol{X}} + \dot{\hat{\boldsymbol{x}}} = \big[(-\boldsymbol{A_1} + \boldsymbol{A_2} + \boldsymbol{A_4}) + \\ + (K + \hat{k})(2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4})\big](\boldsymbol{X} + \hat{\boldsymbol{x}}) \\ + \boldsymbol{B}(\boldsymbol{U} + \hat{\boldsymbol{u}}) \end{aligned} \tag{41}$$

Considering steady state, the values from the state variables are constant, and consequently, the state vector derivative is zero. Thus resulting in the following equations:

$$\dot{\boldsymbol{X}} = 0 \tag{42}$$

$$0 = \boldsymbol{A}\boldsymbol{X} + \boldsymbol{B}\boldsymbol{U} \tag{43}$$

$$\boldsymbol{X} = -\boldsymbol{A^{-1}}\boldsymbol{B}\boldsymbol{U} \tag{44}$$

Therefore, it is possible to obtain (45) when considering that the variation of the mean value is null, as shown in (42), and considering that the product of the two perturbations are minute, that is $\hat{\boldsymbol{x}}\hat{k} << 1$.

$$\begin{aligned} \dot{\hat{\boldsymbol{x}}} = \big[(-\boldsymbol{A_1} + \boldsymbol{A_2} + \boldsymbol{A_4}) + K(2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4})\big]\hat{\boldsymbol{x}} \\ + (2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4})\boldsymbol{X}\hat{k} + \boldsymbol{B}\hat{\boldsymbol{u}} \\ = \boldsymbol{A_n}\hat{\boldsymbol{x}} + \boldsymbol{B}\hat{\boldsymbol{u}} + \boldsymbol{F}\hat{k} \end{aligned} \tag{45}$$

Assuming $\boldsymbol{A_n} = \big[(-\boldsymbol{A_1} + \boldsymbol{A_2} + \boldsymbol{A_4}) + K(2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4})\big]$ and $\boldsymbol{F} = (2\boldsymbol{A_1} - \boldsymbol{A_2} - \boldsymbol{A_4})\boldsymbol{X}$ and also that the AC component of the duty cycle $\hat{k}$ is a new input of the system it is possible to incorporate it on the input matrix, resulting in a new matrix $\boldsymbol{B'} = \big[\boldsymbol{B} \;\; \boldsymbol{F}\big]$, as shown in:

$$\dot{\hat{\boldsymbol{x}}} = \boldsymbol{A_n} + \big[\boldsymbol{B} \;\; \boldsymbol{F}\big]\begin{bmatrix} \hat{\boldsymbol{u}} \\ \hat{k} \end{bmatrix} = \boldsymbol{A_n}\hat{\boldsymbol{x}} + \boldsymbol{B'}\hat{\boldsymbol{u}}' \tag{46}$$

Applying the Laplace's Transform in (46) and, regarding its terms, we obtain (47):

$$\begin{cases} \dot{\hat{\boldsymbol{x}}} = \boldsymbol{A_n}\hat{\boldsymbol{x}} + \boldsymbol{B}^{'}\hat{\boldsymbol{u}}^{'} \\ s\hat{\boldsymbol{x}} = \boldsymbol{A_n}\hat{\boldsymbol{x}}(\boldsymbol{s}) + \boldsymbol{B}^{'}\hat{\boldsymbol{u}}^{'} \\ \hat{\boldsymbol{x}}(\boldsymbol{s})(s\boldsymbol{I} - \boldsymbol{A_n}) = \boldsymbol{B}^{'}\hat{\boldsymbol{u}}^{'} \\ \hat{\boldsymbol{x}}(\boldsymbol{s}) = (s\boldsymbol{I} - \boldsymbol{A_n})^{-1}\boldsymbol{B}^{'}\hat{\boldsymbol{u}}^{'} \end{cases} \tag{47}$$

Considering only the transfer functions where the input is the fluctuation of the duty cycle around the linearized point, it is necessary to consider $\hat{\boldsymbol{u}} = 0$, thus its found:

$$\hat{\boldsymbol{x}}(\boldsymbol{s}) = (s\boldsymbol{I} - \boldsymbol{A_n})^{-1}\boldsymbol{F}\hat{\boldsymbol{k}} \tag{48}$$

The output voltage, described by (49) and the inductor current, described by (50), are found through the linear combination of the variables of the state vector with output matrix $\boldsymbol{C_v}$, (51), and $\boldsymbol{C_i}$, (52), with $\boldsymbol{D} = 0$.

$$\hat{v}_{Co}(s) = \boldsymbol{C_v}\hat{\boldsymbol{x}}(\boldsymbol{s}) \tag{49}$$

$$\hat{i}_L(s) = \boldsymbol{C_i}\hat{\boldsymbol{x}}(\boldsymbol{s}) \tag{50}$$

$$\boldsymbol{C_v} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \tag{51}$$

$$\boldsymbol{C_i} = \begin{bmatrix} 1 & 1 & 0 \end{bmatrix} \tag{52}$$

Thus, it is possible to acquire the output voltage and input current as functions of duty cycle:

$$G_v(s) = \frac{\hat{v}_{Co}(s)}{\hat{k}(s)} = \boldsymbol{C_v}(s\boldsymbol{I} - \boldsymbol{A_n})^{-1}\boldsymbol{F} \tag{53}$$

$$G_i(s) = \frac{\hat{i}_L(s)}{\hat{k}(s)} = \boldsymbol{C_i}(s\boldsymbol{I} - \boldsymbol{A_n})^{-1}\boldsymbol{F} \tag{54}$$

6 IBC control analysis

This section presents the control analysis, PI (Proportional Integral) controllers were chosen once its performance was considered satisfactory for the IBC. The selected topology and its analysis are based on the model proposed by (Fuzato et al., 2018) and (Aguiar, 2017) and it is shown in Figure (10).

The first controls the inductors currents (PI_i) and the second one controls the dc link voltage (PI_v), also providing its output as a reference for the first one.

There are several methods to design the controllers of a system. For this project, the Simulink was used in order to compute the controller gains based in the control diagram and in its specified cut frequencies.

The Figure (11) and (12) show the bode plot with the stability margins of the transfer function in open loop and closed loop as described in the following equations:

$$\hat{i}_L(s) = PI_i(s)\boldsymbol{G_i}(\boldsymbol{s})\boldsymbol{C_i}H_i \tag{55}$$

$$\frac{\hat{i}_L(s)}{\hat{i}_{L\_ref}(s)} = \frac{PI_i(s)\boldsymbol{G_i}(\boldsymbol{s})\boldsymbol{C_i}H_i}{1 + PI_i(s)\boldsymbol{G_i}(\boldsymbol{s})\boldsymbol{C_i}H_i} \tag{56}$$

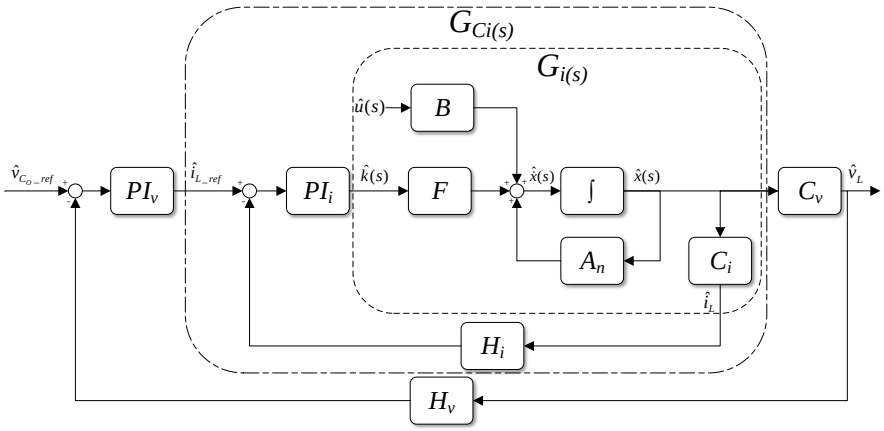

Fig. 10 Diagram of the proposed control model for the converter.

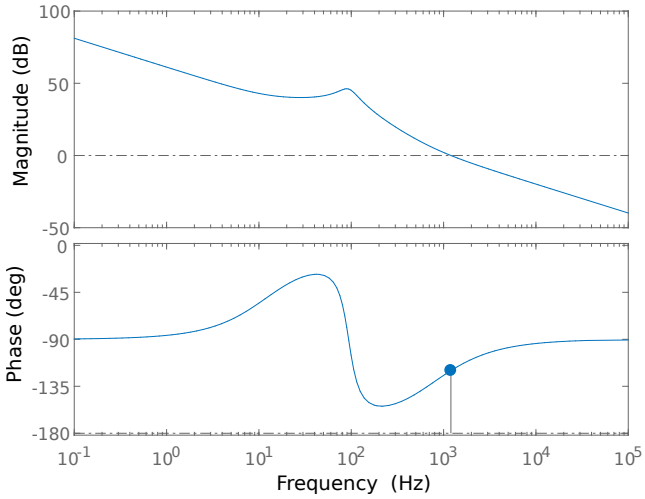

Fig. 11 Bode plot of the open loop current control

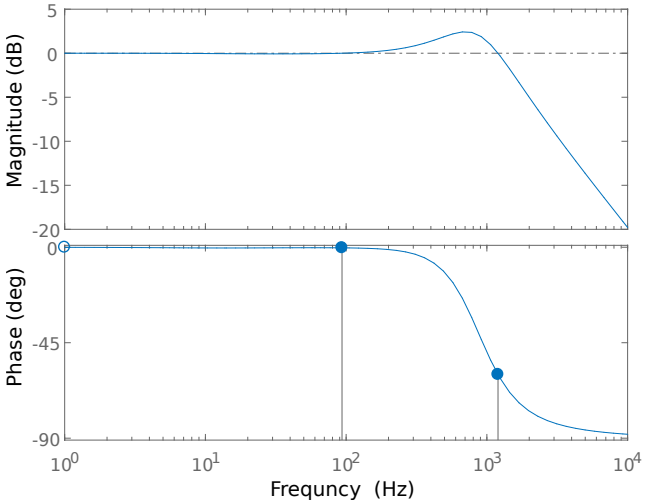

Fig. 12 Bode plot of the closed loop current control

The inner loop transfer function can be acquired starting in (57), that was taken from analysing the topology. Assuming that the input AC variation be null ($\hat{\boldsymbol{u}} = 0$) and applying Laplace, it is found the equation (58).

$$\hat{\dot{\boldsymbol{x}}} = \boldsymbol{A_n}\hat{\boldsymbol{x}} + \boldsymbol{B}\hat{\boldsymbol{u}} - PI_i\boldsymbol{F}H_i\boldsymbol{C_i}\hat{\boldsymbol{x}} + \hat{i}_{L\_ref}PI_i\boldsymbol{F} \tag{57}$$

$$\frac{\hat{\boldsymbol{x}}(\boldsymbol{s})}{\hat{i}_{L\_ref}(s)} = \boldsymbol{G_{Ci}(s)} = (s\boldsymbol{I} - \boldsymbol{A_n} + PI_i\boldsymbol{F}H_i\boldsymbol{C_i})^{-1}PI_i\boldsymbol{F} \tag{58}$$

Thus, it is also possible to analyse the frequency response of the controller in open and closed loop in the subsequent figures and equations:

$$\hat{v}_{Co}(s) = H_vPI_v(s)\boldsymbol{C_v}\boldsymbol{G_{Ci}(s)} \tag{59}$$

$$\frac{\hat{v}_{Co}(s)}{\hat{v}_{C_{o\_ref}}(s)} = \frac{H_vPI_v(s)\boldsymbol{C_v}\boldsymbol{G_{Ci}(s)}}{1 + H_vPI_v(s)\boldsymbol{C_v}\boldsymbol{G_{Ci}(s)}} \tag{60}$$

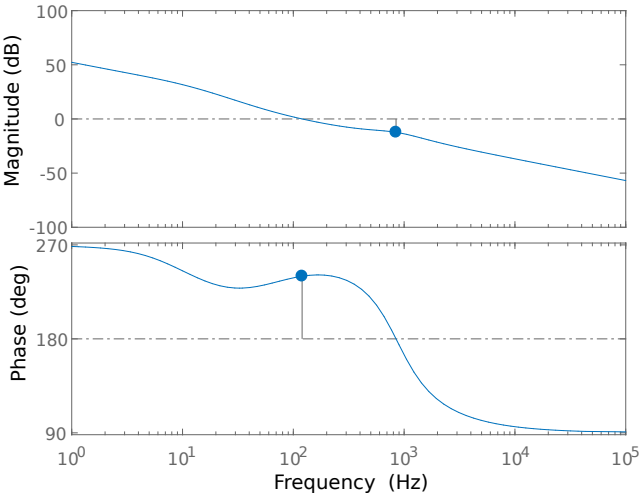

Fig. 13 Bode plot of the open loop voltage control

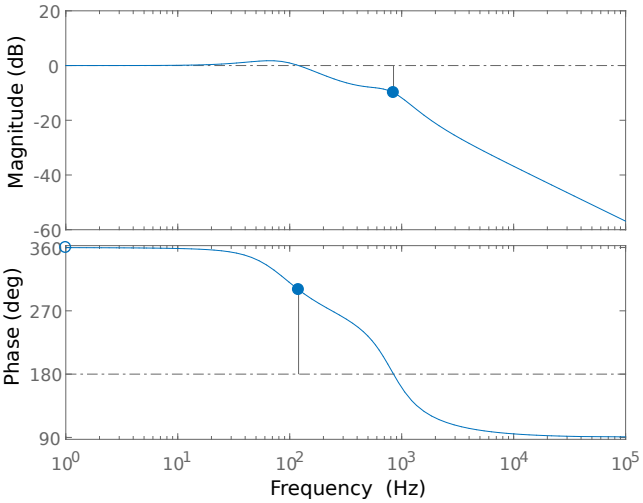

Fig. 14 Bode plot of the closed loop voltage control

The Table 1 specifies the Parameter utilized while performing the control design.

Table 1. Control design specification.

Parameter	Value
Sampling Frequency	12.0 kHz
Cut-off PI_i Frequency	1.2 kHz
PI_i Phase Margin	60°
Cut-off PI_v Frequency	120.0 Hz
PI_v Phase Margin	60°
Hi	1/32
Hv	1/400

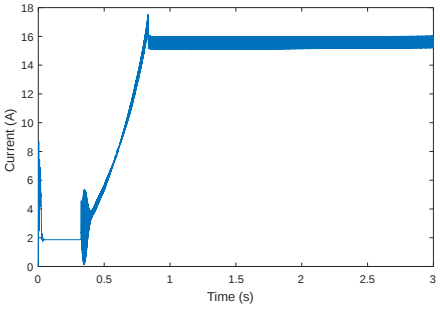

Fig. 16 Current input of the simulated converter.

7 Simulated results

The circuit haiming at the validation of the proposed topology and also to demonstrate its effectiveness and robustness. The software *PSIM* is utilized to build the simulation, and is used an DSP (programmed in C), containing the controllers in discrete form with a sampling rate of 12 kHz. The parameters of the circuit are listed in Table 2.

Table 2. Circuit parameters

Parameter	Value
L_1, L_2	200 mH
R_{L_1}, R_{L_2}	192 mΩ
R_{S_1}, R_{S_2}	28 mΩ
C_{in}	1.270 mF
$R_{C_{in}}$	9 mΩ
C_o	0.4 mF

The next figure shows the current ripple on stationary state. It was possible to observe that this ripple does not surpass 6% of the average current value.

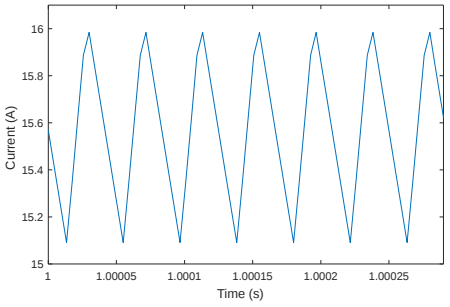

Fig. 17 Current input ripple of the simulated converter.

The converter utilizes a soft startup procedure, through a ramp input function. In the following figures, (15) and (16), it is shown the output voltage response of the described startup and the input current respectively, in both figures the ramp initialization function is easily noted.

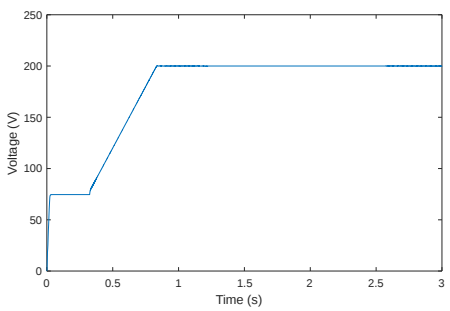

Fig. 15 The simulated converter.

In another instant of the simulation, at 2.095s, the load changes from 1 kW to a third of its value (333 W). The Figure (18) exhibits the output voltage response and the Figure (19) the input current response.

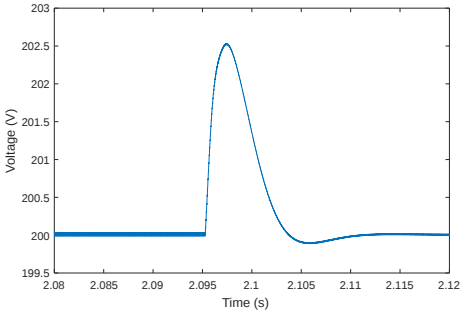

Fig. 18 Output voltage peak on a power drop from 1 kW to 333 W.

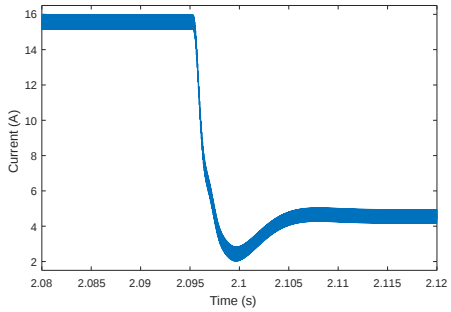

Fig. 19 Input current peak on a power drop from 1 kW to 333 W.

Analysing both figures it was possible to observe that the voltage output has an peak of 1.25% while the input current decays 16% before stabilizing.

Posteriorly, at the instant 2.780 s, the load changes with a step from 333 W to 1 kW. The following figures displays the output voltage response and the input current response respectively.

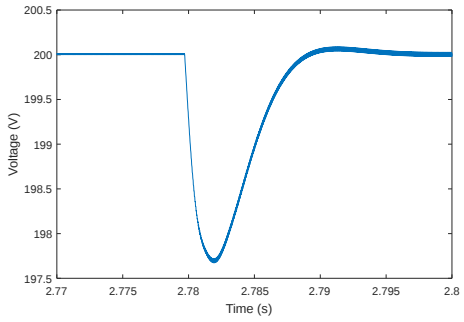

Fig. 20 Output voltage peak on a power step from 333 W to 1 kW.

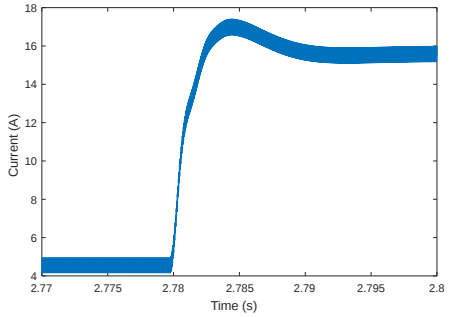

Fig. 21 Input current peak on a power step from 333 W to 1 kW.

Therefore, examining the latter figures, it was possible to observe that the voltage output persists with an error of 1.25% before stabilizing and the current input has an peak of 16% before going back to stabilizing.

8 Experimental results

In order to verify the validity of the IBC, a prototype has been built, Figure (22), to demonstrate the effectiveness of the converter, it uses two switches from the SEMIKRON IGBT Module SK35GD126ET. And the DSP used to control the IBC is the C2000 Delfino MCU F28379D from Texas Instruments.

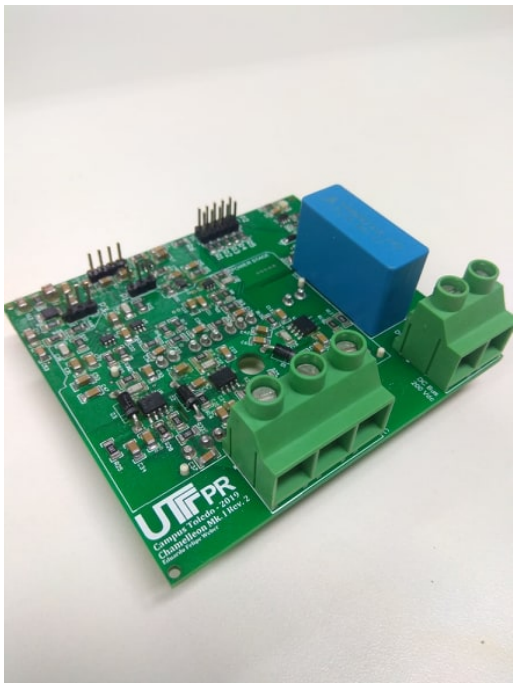

Fig. 22 Printed circuit board prototype.

Because of the laboratory limitations, such as lack of equipment and tools, the prototype was adjusted to process up to 150 W, supplying 100 V on its output, with a 34 V source on its input. Its controllers and feedback gains from table 1 were also tuned to comply with these adjustments.

The switches from the IGBT module are operated through the use of PWM (Pulse Width Modulation), which trigger the gate drivers, controling the switches. In the Figure (23) it is shown the waveform for the gate drives used. The PWM frequency is set to 12 kHz.

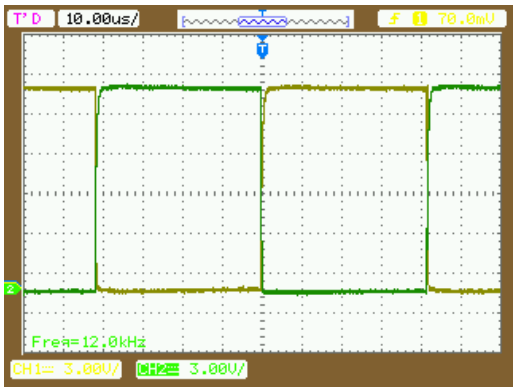

Fig. 23 Gate drivers waveform.

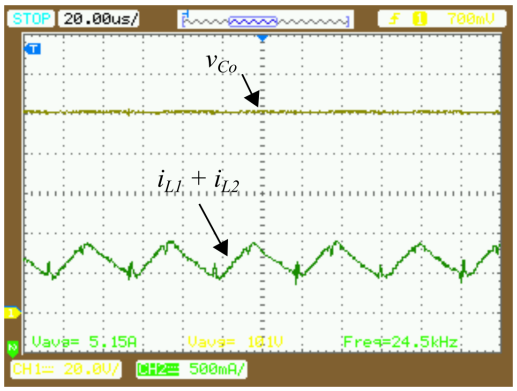

Fig. 25 Prototype stationary state.

Observing the system initialization, Figure (24), it starts with an soft start utilizing a ramp, the same way as in the simulation (figure 15). Aside from the first peak of current ($i_{L1}+i_{L2}$), which is due to the charging of the capacitors, both input current ($i_{L1}+i_{L2}$) and voltage output (v_{C_O}) have none but a small overshoot, not even reaching 1%.

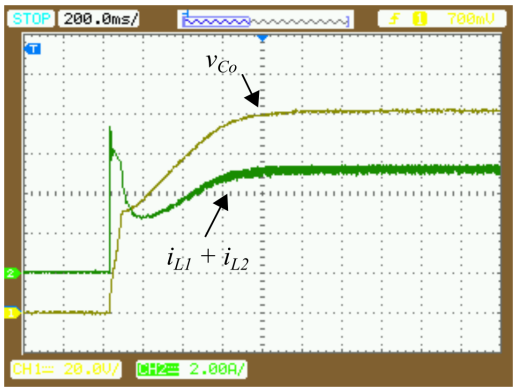

Fig. 24 Prototype initialization.

After the initialization the system goes into stationary state, figure (25), the output voltage (v_{C_O}) shows the effectiveness of the controller as its level is fixed on its designed value having a voltage gain of 2.94. While the input current has a small ripple of less than 4%. Note that, even though the switches operate in 12 kHz the input current ($i_{L1}+i_{L2}$) has a rate of 24 kHz, which is due to the benefit of using the interleaved technique.

In the scenario shown in figure (26), first, the system initializes with a full load and, later on, the load decreases by 50%. Lastly, the load is again increased to 100%.

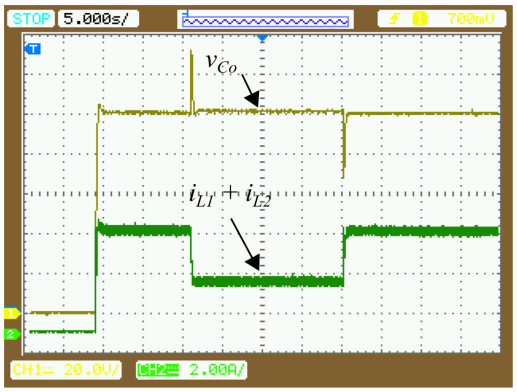

Fig. 26 Response from instant power change.

Going in more detail about this last event, figure (27) shows an image focusing on the instant that the load power drops and the instant that the load goes back to its full value. It is possible to observe that the input current ($i_{L1}+i_{L2}$) shows no overshoot when the load power drops, but display a peak when there is an instant step of power. While the output voltage (v_{C_O}) shows high spikes, in this case of approximately 25%, when any considerably high instant power change happens to the load.

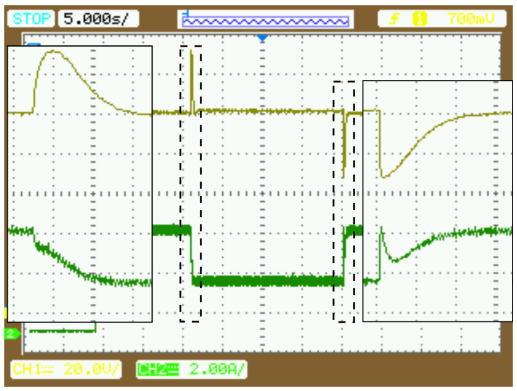

Fig. 27 Response from instant power change detailed.

9 Conclusion

This work presented a two-phase boost interleaved converter, its equations, analysis and control design. Reducing the stress on the semiconductors by the utilization of the interleaved technique as its main feature, a very important factor when utilized on grid-connected systems and uninterruptible applications.

Other important characteristics of the proposed converter are reduced input current ripple, high switching frequency, simple control system, as it uses classical PI controllers.

In contrast, the principal drawbacks of the proposed converter is its duty cycle limitation, it must not be lower than 50%. The converter also requires a soft start and also the current control could be improved to soften its overshoots. There are also some issues with the experimental prototype, principally the high output voltage peak on instant power changes.

Lastly, the proposed converter showed its effectiveness through simulation and experimentation. Still, for future work, it is planned to model parasitic resistances that were ignored and experiment with different kinds of control, such as Fuzzy, to improve its performance.

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